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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Paper No. 17

Application Number: 09/421,437
Filing Date: October 19, 1999
Appellant: CHAPMAN, DAVID C.

Edward A. Becker
For Appellant

EXAMINER'S ANSWER

MAILED
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GROUP 2800

Response to Appellant's Brief filed 25 February 2002.

(1) Real Party in Interest

A statement identifying the real party in interest as David C. Chapman is contained in the brief.

(2) Related Appeals and Interferences

A statement identifying the related appeals and interferences which will directly affect or be directly affected by or have a bearing on the decision in the pending appeal is contained in the brief.

(3) Status of Claims

The statement of the status of the claims contained in the brief is correct.

(4) Status of Amendments After Final

The Appellant's statement of the status of amendments after final rejection contained in the brief is incorrect.

The amendment after final rejection filed on September 10, 2001 has not been entered.

(5) Summary of Invention

The summary of invention contained in the brief is correct.

(6) Issues

The Appellant's statement of the issues in the brief is correct.

(7) Grouping of Claims

Appellant's brief includes a statement that claims 1-6, 10-35, 39-53, and 57-67 do not stand or fall together and provides reasons as set forth in 37 CFR 1.192(c)(7) and (c)(8).

(8) Claims Appealed

The copy of the appealed claims contained in the Appendix to the Brief is correct.

(9) Prior Art of Record

5,550,748	**Xiong**	08-1996

Thorsten Adler et al. (**Adler**), An Interactive Router for Analog IC Design, Proceedings of Design, Automation and Test in Europe, Feb. 1998, pages 414-420.

G. Suzuki et al. (**Suzuki**), A Practical Online Design Rule Checking System, Proceedings., Design Automation Conference, pages 246-252, June 1990.

(10) Grounds of Rejection

The following grounds of rejection are applicable to the appealed claims:

Claims 1-6, 10-20, 22, 24-25, 39-53, and 57-67 are rejected under 35 U.S.C. 103(a) as unpatentable over the Adler paper. **Claim 21** is rejected under 35 U.S.C. 103(a) as unpatentable over the Suzuki paper. **Claim 23** is rejected under 35 U.S.C. 103(a) as unpatentable over Xiong '748. The rejection of claims, 1-6, 10-25, 39-53 and 57-67 are set forth in the Final Office Action, Paper No. 12, and the pertinent rejections are incorporated herein. The Remarks section of the Final Office Action provides additional supporting rationale for the sustained rejections. The pertinent sections of the Final Office Action follow:

DETAILED ACTION

Applicant's Amendment and Response to application, serial number 09/421,437, has been examined and reviewed. Claim 35-67 are added. Claims 11, 12, 24 and 29 are amended. Claims 1-67 are pending.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Rejection of Claims 1-6, 10-20, 22, 24-34

2. **Claims 1-6, 10-20, 22, 24-35, 39-53, 57-67** are rejected under 35 U.S.C. 103(a) as being unpatentable over the Thorsten Adler et al. paper ("the Adler paper") entitled An Interactive Router for Analog IC Design. Adler discloses an interactive two-layer router for an analog integrated circuit. Adler does not use the term "routing indicators" to define the flags which determine routing changes. However, Adler does use tunnel polygons, wave propagation and integer bit flags to control routing layout changes. It would have been obvious to one of ordinary skill in the art at the time of applicant's invention that Adler's methods involve the use of routing controls equivalent to Applicant's routing indicators.

Pursuant to Claim 1 which recites a method for automatically routing an integrated circuit: the Adler paper discloses an interactive, automatic router; Abstract and §1;

receiving integrated circuit layout data that defines a set of two or more integrated circuit (IC) devices to be included in the IC: §2 defines two IC objects, a source (S) and a target (T);

receiving integrated circuit connection data that specifies one or more electrical connection to be made between the IC devices: §3.1, the database contains the connection information;

determining a set of one or more routing indicators that specify a set of one or more preferable intermediate routing locations through which a routing path is to be located to connect first and second IC devices: §3.1 which disclose the integer bits 21 and 29; additionally, this section discloses the use of a flag to indicate acceptable directions;

determining from the IC connection data and the set of one or more routing indicators the routing path between the first and second integrated circuit devices: §3.3 discloses path determination;

updating the IC layout data to generate updated IC layout data that reflects the routing path between the first and second IC devices: §3.4 discloses the updating and generation of final routing path data.

Pursuant to Claim 2, wherein determining the routing path includes determining based upon the IC layout data, the integrated circuit connection data (§2.4 and §3.3), bias direction criteria, §3.4, and straying limit criteria § §3.1-3.4, the routing path between the first and second integrated circuit devices, §3.3.

Pursuant to Claim 3, wherein determining the routing path between the first and second IC includes identifying one or more obstacles that block the routing path: §3.1 discloses obstacle polygons that yields unusable space;

determining indicators that specify one or more preferable routing locations through which the routing path is to be located to avoid the one or more obstacles: §3.4; see also § §3.1-3.3;

determining. . .the routing path between the first and second integrated circuit devices: §3.4.

Pursuant to Claim 4, which recites identifying obstacle that block the routing path: §3.1 discloses the use of obstacle polygons;

changing specified straying criteria. . .: §§2.2 and 2.2.1 discloses routing path widths;

determining. . .the routing path between the first and second integrated circuit devices: §3.4.

Pursuant to Claim 5 which recites identifying obstacle that block the routing path: §3.1 discloses the use of obstacle polygons;

determining a set of one or more layer changes to allow the routing path to avoid the one or more obstacles: §3.1 discloses two level routing and an intermediate layer that Ors together level 1 and level 2 layers;

determining based upon the IC data, the IC connection data, the set of routing indicators, and the set of one or more layer changes, the routing path between the first and second integrated circuit devices: §§3.3-3.4.

Pursuant to Claim 6, which includes the limitation of determining a set of one or more bends to be included in the routing path to avoid the one more obstacle: §2.2.1.

Pursuant to Claim 10, which recites identifying one or more obstacles that block the routing path: §3.1 discloses the use of obstacle polygons;

determining . . . the routing path between the first and second integrated circuit devices: §3.3 discloses path determination.

Pursuant to Claims 11 which includes the additional limitations of determining one or more locations to employ corner clipping to provide additional space for routing the routing path: The Adler paper teaches global and maze routing which suggests corner clipping, and includes design rule modifications and routing paths of various degree angles, §§2.2 and 2.2.1;

Pursuant to Claim 12-14, Adler discloses the additional limitations of determining one or more integrated circuit layout objects to be moved to provide additional space for routing and examining data with layout changes, etc: Adler, §§1-5.

Pursuant to Claim 15, which includes the limitation of determining routing targets: Adler, §§1-5.

Pursuant to Claims 16-20, these claim include the limitation of design rule checking of routing paths and defined attachment or bend angles that are multiples of ninety degrees: Adler, Figs. 1, 2; §§2.1-2.2.2; Abstract.

Pursuant to Claim 22, which includes the limitation of determining. . .a set of two or more join points that are to be electrically connected, wherein each join point from the set of two or more join points has an associated set of specified design criteria that control attachment of routing paths: Adler, §§ 2.2 - 2.4.

Pursuant to Claims 24-28, they address the limitations previously rejected in Claims 1-5, supra and are likewise rejected using the same rationale. Claims 24-28 include the additional limitation of a computer-readable medium having instructions for automatically routing a circuit which is executed by one or more processors. The Adler paper discloses that its method is performed on a Mentor Graphics' ICstation and its

algorithms are implemented using the programming language C++. The Adler paper does not specifically disclose a computer-readable medium but it would have been obvious to one of ordinary skill in the art at the time of applicant's invention that the use of an ICstation would also include the use of computer-readable media as part of the process of implementation. See Adler, §4. Because the Adler paper also addresses the computer-readable media limitation, Claims 24-28 are unpatentable over the Adler paper.

Pursuant to Claims 29-33, they address the limitations previously rejected in Claims 1-5, supra and are likewise rejected using the same rationale. Claims 29-33 include the additional limitation of a system for automatically routing an integrated circuit. This limitation is also addressed by the Adler paper's disclosure of the Mentor Graphics' ICstation.

Pursuant to Claim 34, wherein each routing indicator from the set of one or more routing indicators specifies a routing direction for the routing path: §3.1 discloses an integer value wherein bits 21 to 29 store information about routing direction and bits 31 and 30 are used to mark grid points inside source or target polygons.

Pursuant to Claims 35 and 53, these claims address the limitations already rejected in claim 6 and are likewise rejected using the same rationale. The additional limitation of a computer-readable medium and a system are within the scope of the prior art references which teach CAD systems.

Pursuant to Claims 39 and 57, these claims address the limitations already rejected in claim 10 and are likewise rejected using the same rationale.

Pursuant to Claims 40 and 58, these claims address the limitations already rejected in claim 11 and are likewise rejected using the same rationale.

Pursuant to Claims 41 and 59, these claims address the limitations already rejected in claim 12 and are likewise rejected using the same rationale.

Pursuant to Claims 42 and 60, these claims address the limitations already rejected in claim 13 and are likewise rejected using the same rationale.

Pursuant to Claims 43 and 61, these claims address the limitations already rejected in claim 14 and are likewise rejected using the same rationale.

Pursuant to Claims 44 and 62, these claims address the limitations already rejected in claim 15 and are likewise rejected using the same rationale.

Pursuant to Claims 45 and 63, these claims address the limitations already rejected in claim 16 and are likewise rejected using the same rationale.

Pursuant to Claims 46 and 64, these claims address the limitations already rejected in claim 17 and are likewise rejected using the same rationale.

Pursuant to Claims 47 and 65, these claims address the limitations already rejected in claim 18 and are likewise rejected using the same rationale.

Pursuant to Claims 48 and 66, these claims address the limitations already rejected in claim 19 and are likewise rejected using the same rationale.

Pursuant to Claims 49 and 67, these claims address the limitations already rejected in claim 20 and are likewise rejected using the same rationale.

Pursuant to Claim 50, this independent claims addresses the limitation already rejected in claim 1 and is likewise rejected using the same rationale. The additional

limitation of a computer-readable medium is within the scope of the Adler paper which teaches a Mentor Graphics' IC station.

Pursuant to Claims 51 and 52, these claims address the limitations already rejected by claims 22 and 23, respectively, and are likewise rejected using the same rationale. The additional limitation of a computer-readable medium is within the scope of their respective prior art references which disclose CAD systems.

Rejection of Claim 21

3. **Claim 21** is rejected under 35 U.S.C. 103(a) as being unpatentable over the Suzuki et al. paper ("the Suzuki paper") entitled A Practical Online Design Rule Checking System. The Suzuki paper discloses a method for verifying an IC layout using a design rule checking system. The Suzuki paper's incremental DRC method does not restrict the number of design rule checks to two. However, it would have been obvious to one of ordinary skill in the art at the time of applicant's invention that because the Suzuki paper's incremental DRC method includes the possibility of one or more DRCs, applicant's "second design rule check" limitation is within the scope of the Suzuki paper. Pursuant to Claim 21, Suzuki discloses an automatic, incremental and iterative (to enable a second design rule check) design rule check system, §§2-3.2.

Rejection of Claim 23

4. **Claim 23** is rejected under 35 U.S.C. 103(a) as being unpatentable over Xiong, U.S. patent 5,550,748. Xiong discloses a system and method for delay routing and signal net matching. Xiong does not explicitly teach the step of updating the IC layout data after changes are made. However, it would have been obvious to one of ordinary skill in the art at the time of applicant's invention that the process of routing and

rerouting as disclosed by Xiong would necessarily include updating the IC layout. Pursuant to Claim 23, the limitations of this claims are addressed by Xiong, Figs. 3, 4; Xiong, col. 2, line 44 to col. 3, line 13.

Remarks

Claim 1: Applicant asserts that the prior art does not teach or suggest the limitation " a set of one or more routing indicators that specify a set of one or more preferable intermediate routing locations through which a routing path is to be located": In Adler, the routing indicators are flags and integer bits. According to § 3.1, the bits and the flags determine acceptable directions e.g. which directions are forbidden. Therefore Adler's routing indicators do specify a preferable routing location/direction. The wave, contrary to Applicant's assertions, do determine a path; § 3.3 : "After the wave has reached the target polygon *the path from source to target . . .can be determined.*" Adler also teaches in § 3.3 the limitation "determining from. . .the set of one or more routing indicators. . .the routing path between the first and second integrated circuit devices." § 3.3 discloses the routing of connections between end points. The end points would be considered a first and second integrated circuit devices.

Claim 2: Adler teaches or suggests straying limit criteria and bias direction criteria. In the specification, Applicant states that a straying limit is used to define a region within which a new wire may be routed to connect a starting join point to an ending point. §§3.1-3.4 discusses and illustrates regions of the layout in which new wire may be routed. Applicant's specification also states that a bias direction is used to specify a general direction that a wire should follow during detailed routing to reach a specified

ending join point. § 3.4's Figure 8 in which the wires are routed to the right and to the left suggests bias direction.

Claim 3: The obstacles relate to unusable space and Adler discusses this limitation in § 3.1. Applicant contends that Adler only briefly mentions obstacles. Nevertheless, this is sufficient to satisfy the limitation of identifying one or more obstacles that block the routing path.

Claim 10: Adler identifies obstacles and determines a routing path. This is disclosed in § 3.1.

Claim 16: Applicant states that the limitations of this claim require on-the-fly design rule checking. Examiner does not read this limitation in the claim. Claim 16 merely require design rule checks on routing paths and Adler suggests this limitation by disclosing the existence of special distance rules in the AR router. The distance rules would be the design rules.

Claim 22: Adler discloses connection points which may be considered join points. They are illustrated in Figure 5 and discussed in § 2.4.

Claim 21: Suzuki discloses in § 2.1 that each time an incremental DRC is run, a selected design rule may be set on or off for the particular DRC run. So, the design rule values are *changed* from one design rule check to another depending on what design rule is selected. Examiner therefore maintains the rejection of this claim as obvious over the Suzuki reference.

Claim 23: The limitation "determining whether the distance to be routed for a portion of the routing path exceeds a specified distance, and if the distance to be routed for the

portion of the routing path does not exceed the specified distance, then routing the portion of the routing path in a single step" is suggested in Xiong, col. 2, line 44 to col. 3, line 13. Xiong teaches setting a "net length constraint to the length of a longest routed path." This constraint addresses the "specified distance" limitation. Nets are then rerouted in accordance with net length constraint. Based on the foregoing, Examiner maintains the rejection of Claim 23 as obvious over Xiong.

Claims 24-28: These claims address limitations previously rejected in Claims 1-5, supra. Examiner maintains the rejection of these claims using the same rationale.

Claims 29-33: These claims address limitations previously rejected in Claims 1-5, supra. Examiner maintains the rejection of these claims using the same rationale.

Claim 34: This claim addresses limitations previously rejected in Claim 1. Examiner maintains the rejection of this claim using the same rationale.

Conclusion

5. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

(11) Response to Argument

Introduction

This Examiner's Answer maintains the assertion that Appellant's rejected claims are unpatentable over the prior art. The Final Office Action dated 11 July 2001, a copy of which is incorporated, supra, details the basis for each claim rejection with supporting citations using the respective prior art references. Further detailed discussion of the rejections ensued in the telephonic interview of 27 August 2001 with Appellant and Appellant's representative. Nevertheless, in spite of the evidence of unpatentability presented, Appellant maintains the refrain that "a sufficient factual basis has not been proffered" to support the 35 U.S.C. § 103 rejections. Appellants are not unfamiliar with the prior art references of Adler, Suzuki and Xiong. These references were applied against Appellant's claims in a PCT International Search Report dated 7 March 2000 (Examiner's Answer *Appendix 5*). There, the references were considered as category "X", documents of particular relevance (i.e. the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone). The relevancy of the prior art documents, Adler, Suzuki and Xiong, to the claims of this application remains and Appellant's claims remain unpatentable for the reasons stated herein.

Claims 1-6, 11-15, 19, 20, 24-35, 40-44, 48, 49, 53, 58-62, 66 and 67 are Unpatentable over Adler

Appellant asserts that "Adler does not in any way teach or suggest at least several of the steps required by Claims 1-6, 11-15, 19, 20, 24-35, 40-44, 48, 49, 53, 58-

62, 66 and 67." Brief at page 6. Appellant identifies the first limitation as "determining, based upon the integrated circuit layout data and the integrated circuit connection data, a set of one or more routing indicators that specify a set of one or more preferable intermediate routing locations through which a routing path is to be located" and argues that "[i]n *Adler*, there is no determination of intermediate routing locations or points of any kind through which a routing path is to be located." Brief at page 6.

Routers typically utilize routing indicators to control the location and/or direction of routing paths. The routing indicators take various forms. See, for example, U.S.P. 6,006,024 to Guruswamy et al. (Examiner's Answer *Appendix*) which utilizes a cost metric as a placement quality indicator. *Adler* discloses an interactive router that uses integer bit values to represent layout information. § 3.1, column 1. Of a 32 bit integer value that holds information about the current layout, 9 bits store direction control information. Adler states in part in § 3.1 at paragraphs 3 and 5: Bits 21 to 29 store information whether it's forbidden to extend the wave from the current grid point to the neighbouring grid points. For each forbidden direction a flag is set in the corresponding integer value. In Adler, the wave is used to determine the routing path. If a certain routing path is determined forbidden because of cost, then the pertinent bit in the integer value is set accordingly and the router avoids routing in that prohibited direction.

Appellant's specification details the use of a routing indicator at page 27, lines 9-22. It states in part,

> A simple routing indicator is created and asserted for each new wire during global routing to disable layout changes during detailed routing. If, during global routing existing wires in a particular area need to be moved to allow the routing of a new wire, the simple routing flag is cleared for each routing stretch of the

> affected wires and the nearby portions are rerouted. During detailed routing, the simple routing indicator is examined to determine whether it is set. If so, then during detailed routing, new wires are routed around obstacles, instead of allowing obstacles or surrounding geometry to be modified.

Appellant's routing indicator accomplishes the same purpose as Adler's routing indicator. When set, the routing indicator forbids the routing of wires in a particular circuit area and the routing path must be diverted to some other path. The path could implicitly be determined as "preferable" since the routing indicator by its setting determined that another direction was forbidden. When set, the routing indicator forbids layout changes in a particular area. Adler further at least suggests the presence of intermediate routing locations through which a routing path is to be located. See Adler, § 3.1, column 2, paragraph two, which states in part that "GR's database consists of three levels containing source, target and obstacle polygons: The two routing layers and an intermediate layer used to calculate the via positions during global routing". Adler's Figure 7, illustrated at § 3.1, column 2, and the description of Figure 7 discloses how the intermediate layer is used. However, the presence of intermediate routing locations can also be implied because each point along the way from a source polygon to a target polygon may be considered an "intermediate" point.

Appellant's claim only recites the use of routing indicators that specifies preferable intermediate routing locations. Adler teaches the use of routing indicators which like all routing indicators specify preferable routing locations. Adler's use of the routing indicator to forbid wiring in a certain location, thereby forcing routing in an alternate area indicates a routing preference for some alternate location. Appellant's

use of routing indicators, as disclosed in Appellant's specification at page 27, therefore falls within the scope of Adler's use of routing indicators.

Appellant also mentions that Adler does not teach or suggest the limitation that recites "determining, based upon the integrated circuit layout data, the integrated circuit connection data and the set of one or more routing indicators, the routing path between the first and second integrated circuit devices, wherein the routing path satisfies specified design criteria." This limitation is detailed in Adler at § 3.3, and is firther addressed later in this Answer in response to Appellant's argument.

Claims 10, 29 and 57 are Unpatentable over Adler

Appellant asserts that Claims 10, 29 and 57 are patentable because Adler does not teach the limitation "wherein determining the routing path between the first and second integrated circuit devices includes identifying one or more obstacles that block the routing path, and determining, based upon the integrated circuit layout data, the integrated circuit connection data and the set of one or more routing indicators, the routing path between the first and second integrated circuit devices, wherein the routing path is routed from the second integrated circuit device to the first integrated circuit device." Appellant further asserts that claims 10, 29 and 57 are directed to avoiding obstacles from the second integrated circuit device to the first integrated circuit device. However, the plain language of the claim does not support Appellant's assertion. The language of Appellant's claim is instead particularly directed to a routing path form the first integrated circuit device to the second integrated circuit device. Nevertheless, Adler suggests both routing direction paths.

Appellant's claims first recite "identifying one or more obstacles that block the routing path". This routing path (referencing claim 1 from which claim 10 depends) refers to the path from a first integrated circuit device to a second integrated circuit device. Adler identifies all unusable space which would at least suggest the presence of some type of obstacle. Adler states at page 417, column 2,

> GR's database consists of three levels containing source, target and obstacle polygons. . . This intermediate layer. . .yielding all space not usable. . . .

Next, the claims recite that the routing path between the first and second integrated circuit device is determined. Adler discloses source and target polygons. The source and target, as defined by Adler in § 2, page 414, are two objects between which a connection is made. Appellant's first and second integrated circuit devices are within the scope of Adler's objects, and therefore may be considered as Adler's source and target polygons. Using the GR database, with routing indicators to mark forbidden paths, e.g. paths that contain obstacles, Adler in § 3.1. discloses that a routing path between the source and target is then determined. But, nothing in Adler limits the routing to being unidirectional. In fact, Adler Figure 4, illustrates the interchangeability of source and target. So, a routing path between a second and first integrated circuit device is also within the scope of Adler.

Appellant correctly asserts that Adler discloses Backtracking in §2.3. Backtracking further suggests that routing may also occur from a target to a source, i.e. from a second integrated circuit device to a first integrated circuit device. The Backtracking process examines a path starting at a target cell and ending at a source cell. This procedure is disclosed in detail N. Mani's <u>Optimizing Zig-Zags in Maze-</u>

Routing Algorithm, § 2. Routing Procedure (Examiner's Answer *Appendix*). All of Mani's section 2 should be read in order to properly understand the process. But. the pertinent section of section 2 states in part,

> . . .[T]he backtracking process obtains the shortest path by collecting a set of cells with distinct and decreasing labeling, starting from the target cell and ending at the source cell. When there are multiple choices, the cell whose inclusion in the path does not change the backtrack direction is preferred.

Identifying obstacles is an integral part of any routing process, as disclosed in Adler, irrespective of the routing direction. The cell in the path as referenced in the cited pertinent section represents an identified obstacle which affects the use of that path in the routing process.

Claims 16, 17, 45, 46, 63, and 64 are Unpatentable over Adler

Appellant next asserts that claims 16, 17, 45, 46, 63 and 64 are patentable over Adler because of the limitation "performing one or more design rule checks on one or more portions of the routing path as the routing path is being determined.". However, Adler discloses the use of design rules and design rule modifications in section 2.2 and section 2.2.1. Section 2.2 states in pertinent part,

> The routing algorithm is based on a modification of the well known Lee algorithm which calculates paths of one grid width only. . .This operation guarantees that the calculated one grid path can be replaced by a path of width w without violating the design rules.

This suggests that design rule checks are performed during routing. Furthermore Adler § 2.2.2, it states that "[D]uring sizing it is checked if a new edge intersects with one already created." This sizing procedure occurs during routing and the [design rule] checking therefore occurs during routing. Appellant further states that design rule

checks are performed on an entire layout as a separate phase in layout synthesis. However, routing procedures vary, and one of ordinary skill in the art knows that it is more prevalent to supply a router with design rule criteria and then perform the routing. This would result in continuous checks to ensure that the route meets specified design rule criteria. Adler's design rule checking procedure, broadly interpreted, suggests a continuous checking procedure.

Claims 18, 47, and 65 are Unpatentable over Adler

Appellant next asserts that Claims 18, 47 and 65 are patentable over Adler because of the limitation "extending the routing paths a specified amount to generate an extended portion of the routing path, and selectively performing a design rule check on only the extended portion of the routing path." However, Adler in § 2.4 discloses the avoidance of design rule violations by "*prolongation* of the generated path. . . ." Prolongation of a path means the extension of a path. In Adler, design rule checks are continuously done, therefore performing a design rule check on the extended portion of the routing path would implicitly occur since the prolongation was performed to circumvent a design rule violation.

Claims 22 and 51 are Unpatentable over Adler

Appellant additionally asserts that Claims 22 and 51 are patentable because Adler does not disclose join points associated with a set of specified design criteria that control attachment of routing paths. However, Adler discloses connection points on source and target points and these connection points may be considered to be join points. Adler further discloses in § 2.4: "Design rule violations of type (a) are avoided

by defining connectable points on the edges of S and T." This passage from Adler suggests that the connectable points are defined with consideration of design rule criteria in order to avoid certain violations. Therefore, Adler does read on Appellant's claimed limitation.

Claims 21 and 50 are Unpatentable over Suzuki

Appellant asserts that Claims 21 and 50 are patentable over Suzuki because "Suzuki does not in any way teach or suggest selectively changing one or more values defined by the specified design criteria over time with respect to a layout object and using the changed values in a subsequent design rule check." Brief at page 12. Suzuki teaches incremental design rule checking (DRC) which suggests iteration of layout modification and design rule checking. Suzuki, § 4, page 252 states "In our conventional design, we used the batch type DRC after all the layout design was completed and modified the patterns and ran the DRC again. An average of three to five iterations were made."

Claims 23 and 52 are Unpatentable over Xiong

Appellant asserts that Claims 23 and 52 are patentable over Xiong because "nothing in Xiong in any way teaches or suggests determining whether the distance to be routed for a portion of the routing path exceeds a specified distance, and if the distance to be routed for the portion of the routing path does not exceed the specified distance, then routing the portion of the routing path in a single step." Xiong, in disclosing the process of delay routing states at column 2, lines 53 to 57 states,

> A number of signal nets are matched by setting a net length constraint to the length of the longest routed path, and then rerouting all signal nets using the definition of the search region as the net length constraint.

Xiong's signal nets constitutes a portion of a routing path and the process of setting a net length constraint to the length of the longest routed path falls within the scope of Appellant's limitation of determining whether the distance to be routed for a portion of the routing path exceeds a specified distance. The specified distance is addressed by Xiong's net length constraint. Nets are then routed in accordance with the net length constraint and Xiong, column 2, lines 31-35 suggests that the routing occurs in a single step. Xiong states "It is desirable therefore to provide a delay router that overcomes the limitations of existing routers. Specifically, it is desirable to provide a delay router that provides *complete routing solutions without* extensive CPU time." This passage suggests routing in a single step. Furthermore, one of the prior routing limitations mentioned by Xiong at column 1, lines 56-58 stated that "several routing iterations are needed to achieve a reasonably good result." It would have been obvious to one of ordinary skill in the art that routing in a single step would provide a complete routing solution in a short time frame. Therefore, Xiong at least suggests routing in a single step.

Conclusion

Having considered all of Appellant's arguments, it is respectfully submitted that Appellant's claims 1-6, 10-35, 39-53, and 57-67 are unpatentable over the respective prior art references of Adler, Suzuki and Xiong. Examiner further submits that the rejections have the requisite factual and legal bases; Adler, Suzuki and Xiong teach or at least suggest the argued limitations of Appellant's invention. Accordingly, based on

the foregoing, Examiner respectfully requests that the rejection of claims 1-6, 10-35, 39-53, and 57-67 under 35 U.S.C. § 103(a) as unpatentable over the references cited be **affirmed**.

Respectfully submitted,

A.M. Thompson
Examiner
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May 23, 2002

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PATENT COOPERATION TREATY

PCT

INTERNATIONAL SEARCH REPORT

(PCT Article 18 and Rules 43 and 44)

Applicant's or agent's file reference	FOR FURTHER ACTION	see Notification of Transmittal of International Search Report (Form PCT/ISA/220) as well as, where applicable, item 5 below.
50265-021		
International application No.	International filing date (day/month/year)	(Earliest) Priority Date (day/month/year)
PCT/US 99/24454	19/10/1999	19/10/1998
Applicant		
CHAPMAN, David, C.		

This International Search Report has been prepared by this International Searching Authority and is transmitted to the applicant according to Article 18. A copy is being transmitted to the International Bureau.

This International Search Report consists of a total of 3 sheets.

[X] It is also accompanied by a copy of each prior art document cited in this report.

1. **Basis of the report**

   a. With regard to the **language**, the international search was carried out on the basis of the international application in the language in which it was filed, unless otherwise indicated under this item.

   [ ] the international search was carried out on the basis of a translation of the international application furnished to this Authority (Rule 23.1(b)).

   b. With regard to any **nucleotide and/or amino acid sequence** disclosed in the international application, the international search was carried out on the basis of the sequence listing :

   [ ] contained in the international application in written form.
   [ ] filed together with the international application in computer readable form.
   [ ] furnished subsequently to this Authority in written form.
   [ ] furnished subsequently to this Authority in computer readble form.
   [ ] the statement that the subsequently furnished written sequence listing does not go beyond the disclosure in the international application as filed has been furnished.
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2. [ ] **Certain claims were found unsearchable** (See Box I).

3. [ ] **Unity of invention is lacking** (see Box II).

4. With regard to the **title**,

   [X] the text is approved as submitted by the applicant.
   [ ] the text has been established by this Authority to read as follows:

5. With regard to the **abstract**,

   [X] the text is approved as submitted by the applicant.
   [ ] the text has been established, according to Rule 38.2(b), by this Authority as it appears in Box III. The applicant may, within one month from the date of mailing of this international search report, submit comments to this Authority.

6. The figure of the drawings to be published with the abstract is Figure No. –

   [ ] as suggested by the applicant.
   [ ] because the applicant failed to suggest a figure.
   [X] None of the figures.

INTERNATIONAL SEARCH REPORT

International Application No
PCT/US 99/24454

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 G06F17/50

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 G06F

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	ADLER T ET AL: "An interactive router for analog IC design" PROCEEDINGS. DESIGN, AUTOMATION AND TEST IN EUROPE (CAT. NO.98EX123), PROCEEDINGS DESIGN, AUTOMATION AND TEST IN EUROPE, PARIS, FRANCE, 23-26 FEB. 1998, pages 414-420, XP002132373 1998, Los Alamitos, CA, USA, IEEE Comput. Soc, USA ISBN: 0-8186-8359-7	1,15,19, 20,22, 24,29
Y	abstract paragraphs '0003!,'0005! figures 6-10	2-14, 16-18, 25-33
X	US 5 550 748 A (XIONG XIAO-MING) 27 August 1996 (1996-08-27) column 1, line 64 -column 3, line 13	23

-/--

[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

° Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

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"O" document referring to an oral disclosure, use, exhibition or other means

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Date of the actual completion of the international search	Date of mailing of the international search report
7 March 2000	21/03/2000

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL – 2280 HV Rijswijk	

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication,where appropriate, of the relevant passages	Relevant to claim No.
X	GORO SUZUKI ET AL: "A PRACTICAL ONLINE DESIGN RULE CHECKING SYSTEM" PROCEEDINGS OF THE ACM/IEEE DESIGN AUTOMATION CONFERENCE (DAC),US,NEW YORK, IEEE, vol. CONF. 27, 1990, pages 246-252, XP000245013 ISBN: 0-89791-363-9	21
Y	paragraph '02.1!	16-18
Y	US 5 673 201 A (MALM RICHARD LAVERNE ET AL) 30 September 1997 (1997-09-30) column 2, line 23 -column 3, line 7 column 5, line 22 -column 6, line 3	3-11, 26-33
Y	US 5 258 920 A (HALLER THEODORE R ET AL) 2 November 1993 (1993-11-02) column 6, line 41 - line 63	2,25
Y	US 5 801 960 A (TAKANO MIDORI ET AL) 1 September 1998 (1998-09-01) abstract	12-14
A	WO 93 15471 A (VLSI TECHNOLOGY INC) 5 August 1993 (1993-08-05) abstract	16-18,21

INTERNATIONAL SEARCH REPORT

Inform :on patent family members

Interr nal Application No
PCT/US 99/24454

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 5550748 A	27-08-1996	NONE	
US 5673201 A	30-09-1997	JP 6196563 A	15-07-1994
US 5258920 A	02-11-1993	NONE	
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WO 9315471 A	05-08-1993	US 5450331 A	12-09-1995

OPTIMISING ZIG-ZAGS IN MAZE-ROUTING ALGORITHM

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ABSTRACT

Lee's algorithm for routing finds always a minimum lenghth path, if one exists [1]. We discuss an enhancement to an earlier maze-routing algorithm to reduce the number of zig-zag line segments in the routing path. This method would find a path between two points, if one exists, on a rectangular grid of cells. A line search method using efficient data structures has been applied that would reduce the number of line segments in the path. Blocking cells are introduced as obstacles in finding the path. All line segments are considered as horizontal and vertical only. An implementation of the method and its experimental results are reported.

1. INTRODUCTION

Routing is one of the important phases in printed circuit board (PCB) layout design, physical design of very large scale integrated circuit (VLSI), communication network design and robot navigation [1]. The general routing problem in PCB/VLSI designs can be roughly stated as: Given a set of signal nets each having a number of terminals and a wiring space, connect the pins that belong to the same net together using a limited number of available connection layers such that all the design rules are observed and some other design objective functions are satisfied. Among many objective functions, the most important one is to minimise the wiring length because it affects the circuit performance due to the propagation delay. Though this problem has been studied extensively, it still attracts many researchers

A number of attempts have been made to automate it. Due to the complexity of the routing procedure, routing is separated into many steps. The first step defines rectangular areas called routing channels through which nets are routed, and determines the order in which these channels should be routed. The second step, called global routing or loose routing, assigns a generalised path to each connection within the routing channel, taking into account the wiring length and the congestion created by previously assigned net. Most global routing schemes are based on finding, for each net, a minimal rectilinear path.. The third and final step, called detailed routing, involves determining the unique path for all nets within each of the globally assigned routing channels. The maze-routing algorithm, which is also well known as the Lee's algorithm [1] is a detailed routing scheme. It is one of the oldest method for finding paths in rectangular grids, particularly those involved in printed circuit board (PCB) wiring. In fact, most of the routing algorithm in this field are variants or extensions of the Lee algorithm. [2, 3, 4].

The reasons for the popularity of Lee algorithm are:

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(i) it will always finds a path if one exists; and
(ii) the path it finds will always have the minimum possible length.
However, its exhaustive searching nature makes it slow, especially when the problem size is large. Enhancements were proposed to speed up the search process [5, 6] and parallelize the execution of the algorithm [7, 8, 9, 10, 11,12] In this paper, we discuss one such enhancement to our maze-routing algorithm that reduces the number of zig-zag line segments in its path.

2. ROUTING PROCEDURE

To make the paper more precise, we give some definitions:
Net: A set of pins (or terminals) to be connected.
Horizontal (or vertical) segments : A piece of wire running horizontally (or vertically) on a layer described by two end points.
Route or path: A set of horizontal and vertical segments which implements all or part of a net.

For simplicity in routing and verification of design, routing topologies have been traditionally restricted to Manhattan (or rectilinear) topologies using only horizontal and vertical wires.

The algorithm deals with single layer routing problem on a planer rectangular grid. Its purpose is to find the shortest path between two cells, namely the "*source cell*" and the "*target cell*", on a grid of cells. Some cells are occupied by other circuitry and hence they are not available for routing. They are called "*blocking cells*". The remaining cell are empty, which are called "*free cells*" and hence are available for routing. All the routing line segments are considered as horizontal and vertical only.

The algorithm consists of three phases, namely:

1) Search wave expansion,
2) Backtracking and
3) Label clearance.

Initially, the source cell is labelled as "-2", the target cell is labelled as "-3" and all the blocking cells are labelled as "-1". All the free cells are labelled as "0". In the wave expansion phase, a simulated "search wave" is propagated from the source cell in all the four directions ("north", "east", "south", "west") until the target cell is reached or the wave is unable to expand further.

During the wave expansion phase, all the free cells next to the source cell are labelled as "1", then all the empty cells next to those labelled as "1" are labelled as "2" and so on. If the "search wave" could not reach the target cell, then we conclude that there is no path between the source cell and the target cell. If the "search wave" reached the target cell, then a path can be found by performing the second phase, namely the backtracking.

The backtracking process obtains the shortest path by collecting a set of cells with distinct and decreasing labelling, starting from the target cell and ending at the source cell. When there are multiple choices, the cell whose inclusion in the path does not change the backtrack direction is preferred.

The label clearance phase clears the labels of all the unused cells and makes all the used cells as blocking cells for the routing of the subsequent nets.

A pseudo-code of the recursive procedure Maze for finding the path is given below:

procedure *Router*(source cell coordinates, target cell coordinates)

WHILE the target cell is not reached

DO
BEGIN
Phase-1:
    Starting from the source cell, choose the direction of the move towards the target cell as the one which has larger x difference (or) y-difference between the source cell and the target cell.

Phase-2:
    IF adjacent cell in the direction of move is a free cell **THEN**

        BEGIN
        Move from the start point one unit;

Make the previous points as non-available cells by labelling them appropriately' as the movement is towards "north", "east", "south" or "west" respectively;
Call the procedure *Router*
END
ELSE
BEGIN
Make the direction of movement + 90 degree to the previous direction;
Call the procedure *Router*
END
END
DONE

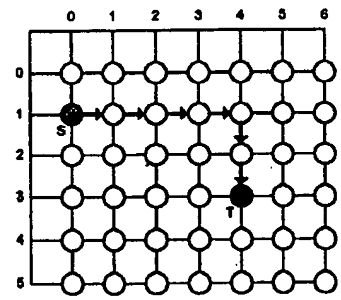
3. DATA STRUCTURE AND IMPLEMENTATION

A linked list data structure is used to store the end points of the line segments of the routing path. From each vertex, there are four possible directions of travel and a priority sequence number is assigned for the direction. The data structure contains an array of pointers to structures consists of x-coordinate and y-coordinate values and members for efficient execution of the program. The line segments of the path are stored in the structure.

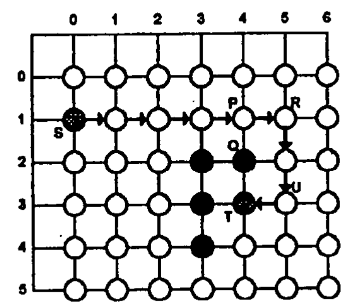
The algorithm has been coded in a PC environment using C++ programming language. The program prompts the user to enter the grid size as:
X dimension: 30
Y dimension: 20

This would generate a rectangular grid of size (30 X 20) for the routing plane. All the cells on the edge of the rectangular grid are considered as blocking cells. Also the user can input a set of blocking cells. These blocking cells represent the already placed component or the earlier routed line connection. The grid size of the routing plane could be changed by giving different X dimension and Y dimension values. The path obtained using the algorithm for three examples are shown.

Example-1:
Source cell: 'S'; Target cell: 'T'; Blocking cells are shown in dark circles.



Example-2



Example-3

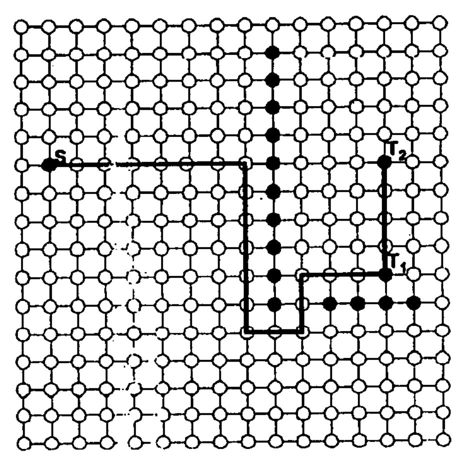


Fig.1 The routing path for the Examples

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